WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a vertical FET access transistor array formed into the depth of a substrate in active webs which run parallel in the lateral direction of the integrated circuit and are implemented as vertical trenches;

an array of storage capacitors, wherein each storage capacitor is associated with a vertical FET access transistor and is formed in a deep trench on a face of a section of an active web which forms the vertical FET access transistor;

a series of wordlines arranged along the active webs;

a series of bitlines intersecting the wordlines;

and an array process diagnosis test structure, wherein the process diagnosis test structure is connected to the wordlines and wherein the connection to the wordlines forms a wordline comb structure.

2. The integrated circuit of claim 1, wherein the process diagnosis test structure is connected to the bitlines and wherein the connection to the bitlines forms a bitline comb structure.

3. The integrated circuit of claim 1, wherein the comb structure comprises:

a first wordline comb connected by a series of contacts to a first series of non-adjacent wordlines along a first edge of the transistor array, wherein the spacing between each successive wordline in the first series of non-adjacent wordlines is defined by a parameter n;

a second wordline comb connected by a series of contacts to a second series of non-adjacent wordlines along a second edge of the transistor array opposite to the first edge, wherein

the spacing between each successive wordline in the second series of non-adjacent wordlines is defined by the parameter n, and wherein the first series and second series of wordlines are offset such that no wordlines are common to both the first and second series.

4. The integrated circuit of claim 3, wherein each contact in the first series of contacts to the first series of wordlines is connected to an area of the active web associated with the respective word line, but is isolated from other elements in the integrated circuit, and

wherein each contact is connected to the comb structure by means of a section of a metal plane.

5. The integrated circuit of claim 4, wherein the section of a metal plane resides in an M0 metal level.

6. The integrated circuit of claim 2, wherein the bitline comb structure comprises:

a first bitline comb connected to a first series of non-adjacent bitlines along a third edge of the transistor array, wherein the spacing between each successive bitline in the first series of non-adjacent bitlines is defined by a parameter m;

a second bitline comb connected to a second series of non-adjacent bitlines along a fourth edge of the transistor array opposite to the third edge, wherein the spacing between each successive bitline in the fourth series of non-adjacent bitlines is defined by the parameter m, and wherein the first series and second series of bitlines are offset to include no common bitlines.

7. The integrated circuit of claim 3, further comprising a bitline comb, wherein the bitline comb structure comprises:

a first bitline comb connected to a first series of non-adjacent bitlines along a third edge of the transistor array, wherein the spacing between each successive bitline in the first series of non-adjacent bitlines is defined by a parameter m;

a second bitline comb connected to a second series of non-adjacent bitlines along a fourth edge of the transistor array opposite to the third edge, wherein the spacing between each successive bitline in the fourth series of non-adjacent bitlines is defined by the parameter m, and wherein the first series and second series of bitlines are offset to include no common bitlines.

8. The integrated circuit of claim 3, wherein the value of n is equal to 2.

9. The integrated circuit of claim 6, wherein the value of m is equal to 2.

10. The integrated circuit of claim 7, wherein the value of n is equal to 2, and wherein the value of m is equal to 2.

11. The integrated circuit of claim 3, wherein value of n is equal to 4,

wherein the mutual offset between the first and second wordline combs is two wordlines,

further comprising a wordline meander, wherein, by means of a series of contacts, the wordline meander connects in series all of the worldines that lie between the wordlines that are connected to the first and second wordline combs, such that the wordline meander is isolated from the first and second wordline combs.

12. The integrated circuit of claim 10, wherein each pair of successive wordlines in the wordline meander are linked by a U-shaped section of a metal plane connected to each contact of the pair of successive wordllines.

13. The integrated circuit of claim 11, wherein the U-shaped section resides in an MO metal plane level.

14. The integrated circuit of claim 7, wherein value of n is equal to 4,

wherein the mutual offset between the first and second wordline combs is two wordlines,

further comprising a wordline meander, wherein, by means of a series of contacts, the wordline meander connects in series all of the worldines that lie between the wordlines connected to the first and second wordline combs, such that the wordline meander is isolated from the first and second wordline combs.

15. The integrated circuit of claim 7, wherein value of m is equal to 4,

wherein the mutual offset between the first and second bitline combs is two bitlines,

further comprising a bitline meander, wherein the bitline meander connects in series all of the bitlines that lie between the bitlines connected to the first and second bitline, combs such that the bitline meander is isolated from the first and second bitline combs.

16. The integrated circuit of claim 15, wherein the bitline meander comprises a section of metal formed in an M0 metal level.

17. The integrated circuit of claim 2, further comprising a buried drain contact strip formed in a desired region of the transistor array and arranged parallel to the direction of the bit lines, wherein the buried drain contact strip is formed where the layout areas of a deep trench and an active web intersect,

whereby the buried contact strip establishes a contact between a storage capacitor formed in a deep trench, and an associated vertical FET transistor,

and whereby contact between semiconductor memory cells in the desired region and an associated bit line is made.

18. An integrated circuit for testing performance of memory devices comprising:

an array of memory cells wherein each cell includes a vertical FET access transistor and a deep trench capacitor associated with the access transistor;

a series of parallel wordlines for contacting the access transistor gates;

a series of parallel bitlines;

a buried drain contact strip for connecting a bitline to a memory cell;

and a test structure comprising a plurality of comb-like structures, wherein each of a first pair of comb-like structures link a series of regularly spaced non-adjacent wordlines together, wherein the pair of comb-like structures connect to wordlines of the array at opposite edges, and wherein the comb-like structures are mutually offset such that no wordlines are shared between the two comb-like structures.

19. The integrated circuit of claim 18, wherein plurality of comb-like structures further comprises a second pair of comb-like structures linking a series of regularly spaced

bitlines together, wherein the pair of comb-like structures connect to bitlines of the array at opposite edges, and wherein the comb-like structures are mutually offset such that no bitlines are shared between the two comb-like structures.